UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,437	01/22/2004	Sang-Hoon Park	8054-30 (AW8134US/JY)	5190

22150 7590 05/04/2005

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
THOMAS, TONIAE M	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,437	PARK, SANG-HOON	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-21 is/are pending in the application.

4a) Of the above claim(s) 1-8 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 9,15 and 18-21 is/are rejected.

7)☒ Claim(s) 10-14,16 and 17 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 01/22/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 9-21, in the reply filed on 07 April 2005 is acknowledged. Claims 1-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9, 15, 18, 19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zurcher et al. (US 6,500,724 B1) in view of Summerfelt et al. (US 6,635,498 B2).

The Zurcher et al. patent (Zurcher) discloses a method for manufacturing a capacitor in a semiconductor device (fig. 1 and accompanying text). The method comprises: forming a first insulation layer 12 on a substrate 10 (fig. 1 and col. 3, lines 39-53); forming a lower wiring 16 and a lower electrode 16 in the first insulation layer (fig. 1 and col. 3, lines 39-53); forming a dielectric layer 22 on the first insulation layer including the lower wiring and the lower

electrode (fig. 1 and col. 3, line 65 - col. 4, lines 3); forming a conductive layer 24 on the dielectric layer (fig. 1 and col. 4, lines 3-8); forming a first protection layer 26 on the conductive layer (fig. 1. and col. 4, lines 3-8); etching the first protection layer to form a first protection layer pattern (fig. 1 and col. 4, lines 3-8); etching the conductive layer to form an upper electrode on a portion of the dielectric layer positioned on the lower electrode (fig. 1 and col. 4, lines 3-8); forming a second protection layer 30 on the dielectric layer and on the first protection layer pattern (fig. 1 and col. 4, lines 26-30); forming a second insulation layer 34 on the second protection layer (fig. 1 and col. 4, lines 26-30); forming a first contact 40 contacting the lower wiring through the second insulation layer (fig. 1 and col. 3, lines 3-7);[1] forming a second contact 38 contacting the upper electrode 24 through the second insulation layer, the second protection layer and the first protection layer pattern (fig. 1 and col. 3, lines 3-7); and forming a first upper wiring 44 on the first contact, and a second upper wiring 44 on the second contact (fig. 1 and col. 3, lines 3-7).

The second protection layer 30 is formed on the portion of the dielectric layer positioned on the lower electrode, a sidewall of the upper electrode and a sidewall of the first protection layer pattern (fig. 1).

The lower electrode 16 comprises one of copper and aluminum (col. 1, lines 57-64), the upper electrode 24 comprises one of titanium nitride and

[1] First contact 40 is in electrical contact with the lower wiring 16 via resistor 28. The claim language does not recite that the first contact is directly contacting the lower wiring. Therefore, the claim language does not preclude contacting the lower wiring 16 via an intermediate layer.

tantalum nitride (col. 3, lines 22-25), and the dielectric layer 22 comprises one of oxide (e.g. Ta_2O_5, $SrTiO_3$, ZrO_2, $ZrSiO_4$, HfO_2, $HfSiO_4$, TiO_2), nitride (e.g. Si_3N_4), and a composite of oxide and nitride (col. 3, lines 16-22).

As explained above, Zurcher discloses forming a conductive layer 24 on the dielectric layer 22, forming a first protection layer 26 on the conductive layer, etching the first protection layer to form a first protection layer pattern, and etching the conductive layer to form an upper electrode. Zurcher further discloses that blanket deposition techniques may be used followed by one or more patterning steps (Zurcher - col. 4, lines 5-8). However, Zurcher does not explicitly teach etching the first protection layer to form a first protection layer pattern on the conductive layer, and etching the conductive layer using the first protection layer pattern as an etching mask. In addition, Zurcher does not teach that the first and second upper wirings comprise one of copper and aluminum.

Summerfelt teaches etching a first protection layer to form a first protection layer pattern on a conductive layer, and etching the conductive layer using the first protection layer pattern as an etching mask to form an upper electrode. Summerfelt discloses a method for forming a capacitor in a semiconductor device (figs. 3, 6a-6n, and accompanying text). The method comprises: forming a conductive layer 128, 130 on a dielectric layer 126 (fig. 6e and col. 12, lines 45-47), forming a first protection layer 132 on the conductive layer (fig. 6f and col. 13, lines 23-26), etching the first protection layer to form

a first protection layer pattern 132 on the conductive layer (fig. 6g and col. 15, lines 11-17), and etching the conductive layer using the first protection layer pattern as an etching mask to form an upper electrode (fig. 6h and col. 15, lines 11-17). Summerfelt also teaches forming first and second upper wirings 144, wherein the upper wirings comprise one of copper and aluminum (fig. 3 and col. 9, lines 36-41).

Zurcher and Summerfelt are from the same field of endeavor, fabrication methods for forming metal-insulator-metal (MIM) capacitors in semiconductor devices. Thus, the purpose for which Summerfelt is relied upon would have been recognized in the primary reference, Zurcher, by one of ordinary skill in the art at the time the invention was made.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Zurcher by etching the first protection layer to form a first protection layer pattern on the conductive layer and etching the conductive layer using the first protection layer pattern as an etching mask, as taught by Summerfelt, because etching the conductive layer using the first protection layer pattern as an etching mask requires only one masking step. Furthermore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the first and second upper wirings comprising one of copper and aluminum, as taught by Summerfelt, because both copper and aluminum have low resistivity.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zurcher et al. in view of Summerfelt as applied to claim 15 above, and further in view of Huang et al. (US 2003/0232481 A1).

Zurcher does not teach that each of the first protection layer pattern 26 and the second protection layer 30 comprises one of silicon nitride and silicon carbide, as recited in claim 20. However, the Huang et al. patent (Huang) discloses a method for forming a capacitor in a semiconductor device (figs. 1-5 and accompanying text), wherein the method comprises forming a first protection layer 28 on a first conductive layer 26 (fig. 2 and par. 46), etching the first protection layer to form a first protection layer pattern 28a (fig. 3 and par. 50), etching the first conductive layer to form an upper electrode 26a on a dielectric 24a (fig. 3 and par. 50), and forming a second protection layer 30 (fig. 4 and par. 57). Both the first and second protection layers comprise silicon nitride (par. 46 and par. 57).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Zurcher and Summerfelt, by forming the first and second protection layers comprising silicon nitride, as taught by Huang, because silicon nitride provides a diffusion barrier for the lower and upper electrodes (Huang - par. 47, lines 8-15).

Allowable Subject Matter

3. Claims 10-14, 16, and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record does not anticipate, teach or suggest a method for forming a semiconductor device substantially as claimed, wherein the method comprises partially etching the first protection layer and the dielectric layer adjacent the dielectric layer during etching of the conductive layer to form an upper electrode, as recited in claims 10 and 16.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
29 April 2005

Mary Wilczewski
Primary Examiner